

IFW



To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
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Subject: | Serial No. 10/796,427 03/09/04 |

Mou-Shiung Lin et al.

POST-PASSIVATION METAL SCHEME ON
AN IC CHIP WITH COPPER

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

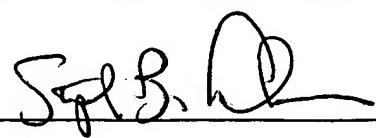
The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on May 24, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 5/24/04

U.S. Patent Application MS-002CCC_CIP, filed 05/24/02, Serial No. 10/154,662, assigned to the same assignee, "Top Layers of Metal for High Performance IC's," discusses the manufacturing of high performance Integrated Circuit (IC's).

U.S. Patent Application MEG-02-016, filed 05/27/03, Serial No. 10/445,558, assigned to the same assignee, "High Performance System-on-Chip Inductor Using Post Passivation," discusses the manufacturing of high performance IC's.

U.S. Patent Application Publication US 2004/0029404 A1 to Lin, "High Performance System-on-Chip Passive Device Using Post Passivation Process," discloses a system and method for forming post passivation passive components, such as resistors and capacitors.

U.S. Patent Application Publication US 2004/0016948 A1 to Lin, "High Performance System-on-Chip Discrete Components Using Post Passivation Process," discloses a system and method for forming post passivation discrete components.

U.S. Patent 6,544,880 to Akram, "Method of Improving Copper Interconnects of Semiconductor Devices for Bonding," discloses gold over a copper pad and optionally additional metals to prevent formation of intermetallic compounds in wire bonding.

The following two U.S. Patents teach using an Al cap over a copper bond pad for wire bonding:

- 1) U.S. Patent 6,451,681 to Greer, "Method of Forming Copper Interconnection Utilizing Aluminum Capping Film".
- 2) U.S. Patent 6,376,353 to Zhou et al., "Aluminum and Copper Bimetallic Bond Pad Scheme for Copper Damascene Interconnects."

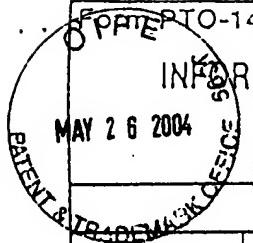
The following two U.S. Patents discloses a post-passivation interconnection process:

- 1) U.S. Patent 6,495,442 to Lin et al., "Post Passivation Interconnection Schemes on Top of the IC Chips."
- 2) U.S. Patent 6,383,916 to Lin, "Top Layers of Metal for High Performance IC's."

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761



PROPERTY-1449

**INFORMATION DISCLOSURE CITATION
IN AN APPLICATION**

MAY 26 2004

(Use several sheets if necessary)

Doctor Number (Optional)

Agricultural Museum

MEG-03-005

101796,427

Applicant

Mou-Shiung Lin et al.

Filing Date

03/09/04

03/09/04

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (*Including Author, Title, Date, Pertinent Pages, Etc.*)

- US Patent App. MSL-98-002ccc CIP, Filed 05/24/02,
Ser # 10/154,662, assigned to the same assignee, "Top
Layers of Metal for High Performance IC's".
 - US Patent App. MEG-02-016, Filed 05/27/03,
Ser. # 10/445,558, "High Performance System-on-Chip
Inductor Using Post Passivation Process".

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

